NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2014-2015

EE2004/IM1004 – DIGITAL ELECTRONICS

November / December 2014 Time Allowed: 2½ hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 7 pages.
2. Answer ALL questions.
3. All questions carry equal marks.
4. This is a closed-book examination.

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1. (a) Simplify the circuit shown in Figure 1 down to its minimum sum-of-products (SOP) form and connect your minimum circuit using the 74LS54 TTL AND-OR-INVERT (AOI) gate and 7404 TTL hex inverter ICs given in Figure 2 on page 2.

(8 Marks)

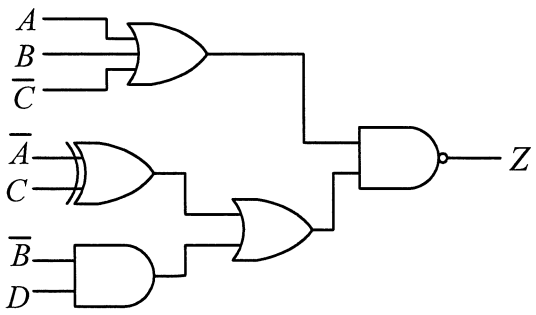

Figure 1

Note: Question No. 1 continues on page 2.

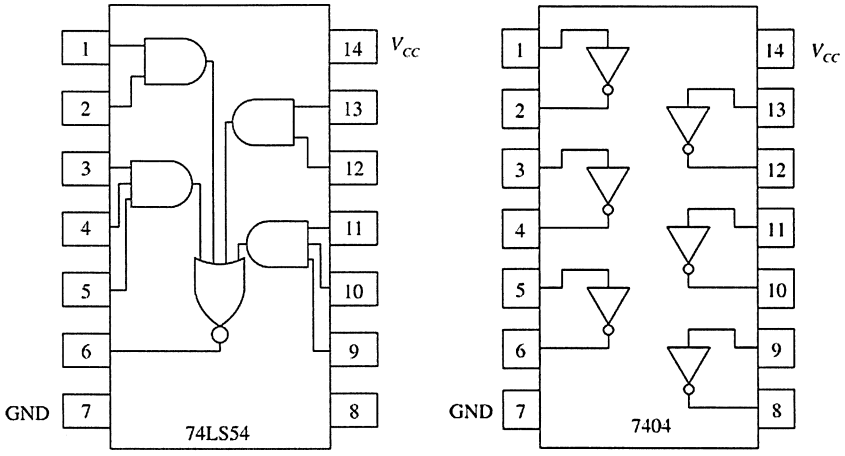

Figure 2

(b) Draw the transistor-level CMOS AOI circuit for the minimum function derived in part (a).

(7 Marks)

(c) List the advantages of CMOS circuits.

(5 Marks)

2. (a) A circuit is designed to receive information in the form of BCD code. The bits it receives are A_3, A_2, A_1, A_0, with A_3 being the MSB. To ensure that the bits received form a valid BCD code (i.e., ≤1001), the circuit includes a BCD error detector circuit that examines the received code. Design the BCD error detector circuit to produce a HIGH for an error condition. Derive the truth table and the minimal function. Draw the logic diagram of the minimal function.

(10 Marks)

(b) The truth table of a 4-bit magnitude comparator is given in Table 1. Design a 6-bit magnitude comparator to compare a binary input ($X_5X_4X_3X_2X_1X_0$) with the binary number (010101_2), using:

(i) **TWO** 4-bit magnitude comparators and basic logic gates such as Inverters, NANDs, NORs, etc., if necessary.

(ii) **ONE** 4-bit magnitude comparator and basic logic gates such as Inverters, NANDs, NORs, etc., if necessary.

(10 Marks)

Table 1 Truth table of 74×85 4-bit magnitude comparator

Input Data				Cascading Inputs			Outputs		
A_3B_3	A_2B_2	A_1B_1	A_0B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$Y_{A>B}$	$Y_{A<B}$	$Y_{A=B}$
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L

3. Analyze the clocked synchronous state machine in Figure 3.

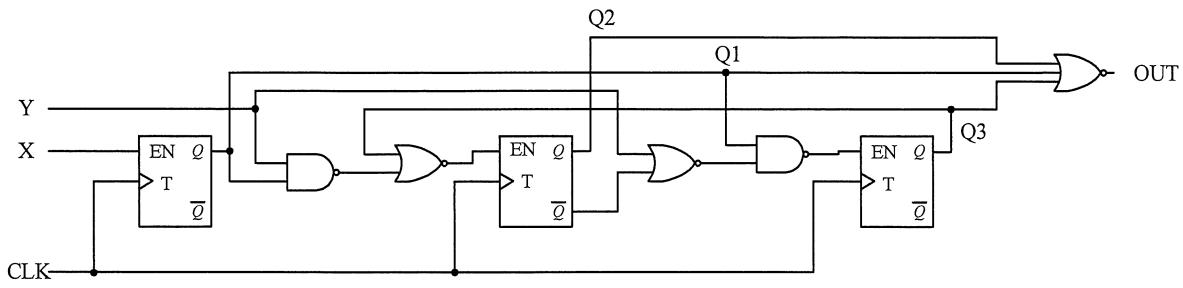

Figure 3 A clocked synchronous state-machine

(a) Determine whether Figure 3 is a Mealy machine or a Moore machine and explain your answer.

(2 Marks)

(b) Write the excitation equations.

(4 Marks)

(c) Write the transition equations.

(4 Marks)

(d) Draw the transition table.

(4 Marks)

(e) Draw the state/output table.

(2 Marks)

(f) Draw the state diagram.

(4 Marks)

4. (a) Table 2 shows the state table of a state machine with single input I. The present state is represented by P. The table entries are of the form N/O, where N denotes the next state and O is the output of the current state. State transitions occur on the rising edges of CLOCK, which have been shown as numbered dashed lines in Figure 4 on page 6. Draw the state diagram.

(5 Marks)

Table 2

	I = 0	I = 1
P	N/O	N/O
0	0/0	1/0
1	1/1	0/1

(b) Complete the timing diagram shown in Figure 4 on page 6 by showing P, N and O. Note that P has an initial value of 0.

(5 Marks)

(c) Implement the state machine using D flip-flop. Show the corresponding sequential circuit diagram.

(5 Marks)

(d) Assume that the above sequential circuit in part (c) can be described as shown in Figure 5 on page 6. The propagation delay of D flip-flop FF1 is t_p and the propagation delay of logic is t_d. For D flip-flop FF2, the setup time is t_s and hold time is t_h. Derive the maximum clock frequency f_{max} that has no timing violation.

(5 Marks)

Note: Question No. 4 continues on page 6.

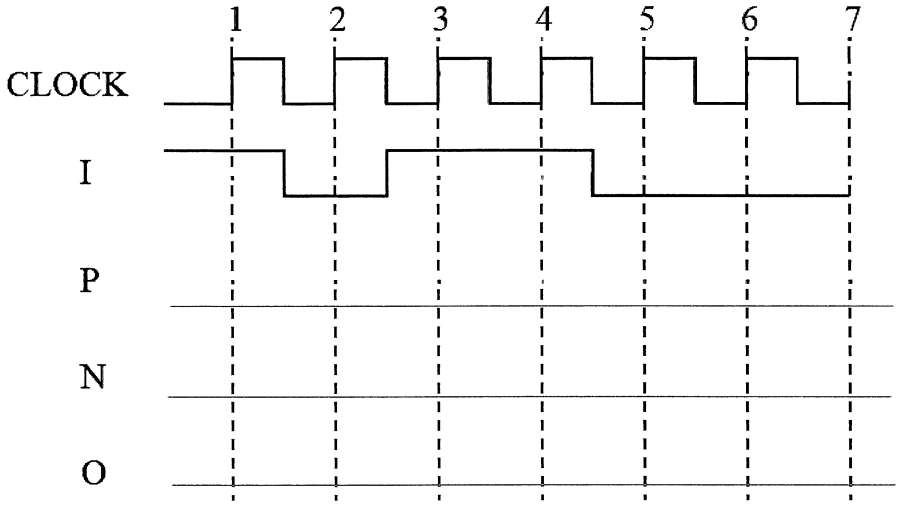

Figure 4

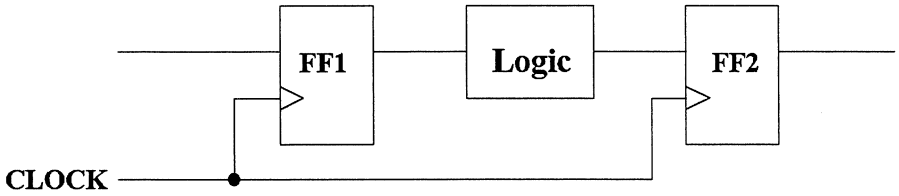

Figure 5

5. (a) Design a 4-bit synchrotrons counter to count the following repeated sequence: 0, 4, 8, 9, 5, 1; 0, 4, 8, 9, 5, 1; … If the counter enters unused states, make sure it will go to state 0 at the next clock cycle. Draw the state diagram.

(4 Marks)

(b) Draw the state transition table when using: (i) D flip-flops; and (ii) T flip-flops.

(4 Marks)

(c) Implement the counter using D flip-flops. Show detailed steps of derivation and the final circuit diagram.

(6 Marks)

(d) Implement the counter using T flip-flops. Show detailed steps of derivation and the final circuit diagram.

(6 Marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.