NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2014-2015

EE2004 / IM1004 – DIGITAL ELECTRONICS

April / May 2015 Time Allowed: 2½ hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 6 pages.
2. Use the separate answer sheets provided for questions 3(a) & 3(b) and attach them to the answer book.
3. Answer ALL questions.
4. All questions carry equal marks.
5. This is a closed-book examination.
6. Unless specifically stated, all symbols have their usual meanings.

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1. (a) Represent -367_{10} in the following number systems with 12 bits and express your answers in hexadecimal.

   (i) Sign and Magnitude Number System.

   (ii) 2's Complement Number System.

   (8 Marks)

   (b) Given a logic function $z(a, b, c, d, e) = b \cdot (e + \bar{d}) \cdot a + c$, derive a CMOS circuit for the function and label the inputs and output clearly.

   (8 Marks)

   (c) The input and output specifications of two logic families EEE01 and EEE02 are given in Table 1 on page 2.

   (i) Determine the fanout for the logic family EEE02.

   (ii) Determine the fanout for an EEE02 gate to drive EEE01 gates.

Note: Question No. 1 continues on page 2.

Table 1

Family	V_{ILmax} (V)	V_{OLmax} (V)	V_{IHmin} (V)	V_{OHmin} (V)	I_{ILmax} (μA)	I_{OLmax} (μA)	I_{IHmax} (μA)	I_{OHmax} (μA)
EEE01	0.6	0.4	1.2	1.6	–13	210	17	–190
EEE02	0.8	0.5	1.4	1.8	–37	490	73	–430

(4 Marks)

2. (a) Derive the minimized sum-of-products (SOP) expression of the following logic function:

$$f(\mathrm{A,B,C,D}) = \Sigma m(0,1,8,11,12,14) + d(3,6,9).$$

(10 Marks)

(b) Find the Maxterms of the logic function $g(a,b,c,d) = \overline{d} \cdot (\overline{a \cdot \overline{c}} + b \cdot \overline{d})$. Express your answer in the format of $g(a, b, c, d) = \Pi M(\ldots)$.

(10 Marks)

3. A_1A_0 and B_1B_0 are two 2-bit binary numbers. Let $Y_{A>B} = 1$ if $A_1A_0 > B_1B_0$, otherwise, $Y_{A>B} = 0$; let $Y_{A=B} = 1$ if $A_1A_0 = B_1B_0$, otherwise, $Y_{A=B} = 0$; and let $Y_{A<B} = 1$ if $A_1A_0 < B_1B_0$, otherwise, $Y_{A<B} = 0$.

(a) Complete the truth-table for $Y_{A>B}$, $Y_{A=B}$ and $Y_{A<B}$ shown in Table 2 of the **answer sheet provided.**

(5 Marks)

(b) Realize the truth-table in PART (a) using a 4-input 3-output PAL given in Figure 1 on page 3. **Note:** Use the answer sheet provided for this part.

(5 Marks)

(c) Realize the truth-table in PART (a) using a 4-bit magnitude comparator 7485. The truth table of the comparator 7485 is given in Table 3 on page 4.

(5 Marks)

(d) Realize the truth-table in PART (a) using two 74151 8-to-1 MUXs or two 3-to-8 binary decoders. Assume that the complements of A_1, A_0, B_1 and B_0 are available and can be used directly in the realization. Additional primitive gates such as AND, NAND, OR, NOR gates and INVERTERs may be used. The truth tables of the modules 74151 and 3-to-8 decoder are given in Tables 4 and 5 on page 4, respectively.

(5 Marks)

Note: Question No. 3 continues on page 3.

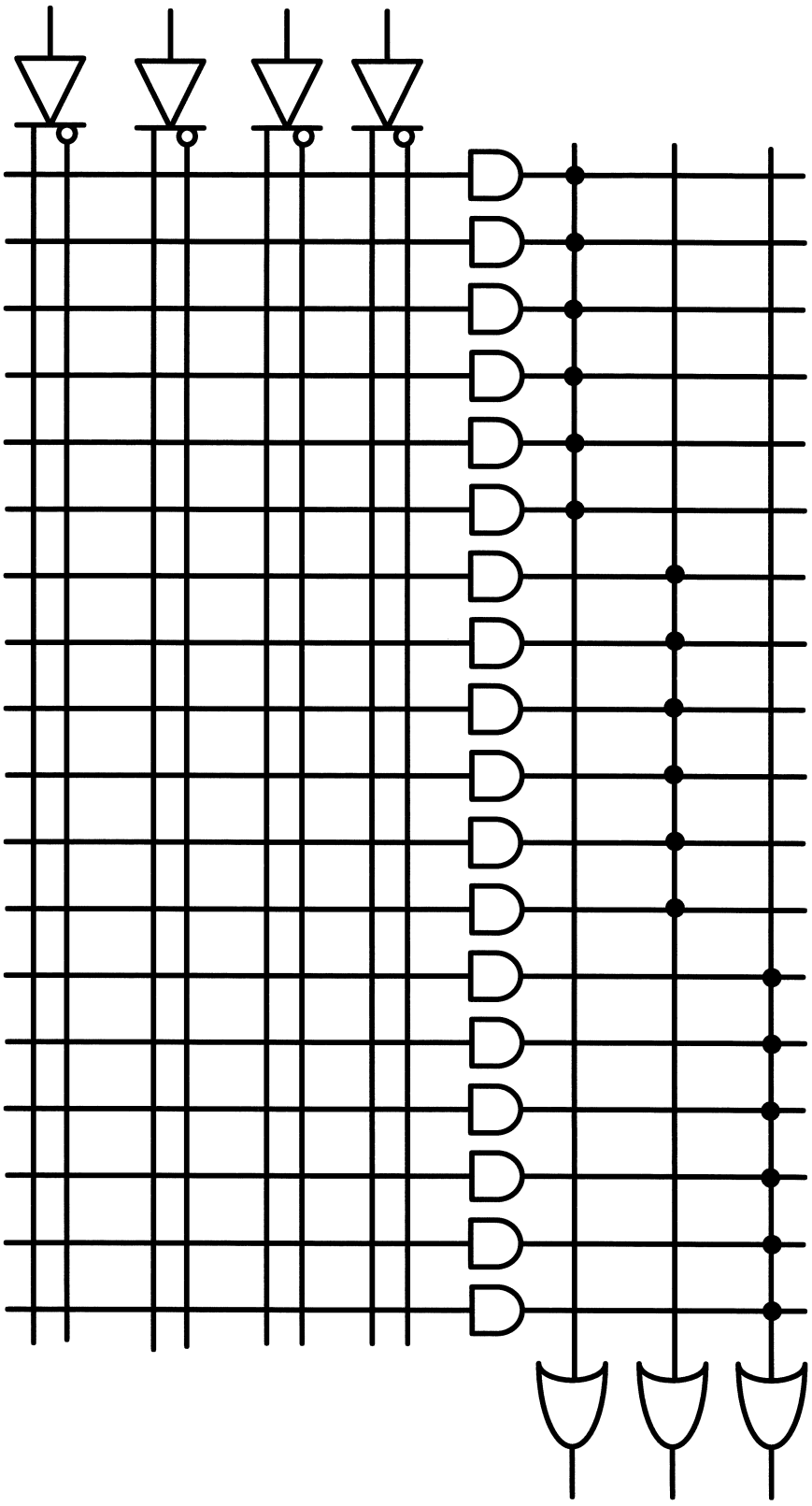

Figure 1

Note: Question No. 3 continues on page 4.

Table 3

Truth-table of Comparator 7485

Input Data				Cascading Inputs			Outputs		
A_3B_3	A_2B_2	A_1B_1	A_0B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$Y_{A>B}$	$Y_{A<B}$	$Y_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L

Table 4

Truth-table of 74151

Inputs Select			Strobe	Outputs	
C	B	A	$\overline{G}$	Y	W
x	x	x	1	0	1
0	0	0	0	D_0	$\overline{D}_0$
0	0	1	0	D_1	$\overline{D}_1$
0	1	0	0	D_2	$\overline{D}_2$
0	1	1	0	D_3	$\overline{D}_3$
1	0	0	0	D_4	$\overline{D}_4$
1	0	1	0	D_5	$\overline{D}_5$
1	1	0	0	D_6	$\overline{D}_6$
1	1	1	0	D_7	$\overline{D}_7$

Table 5

Truth-table of 3-8 decorder

Inputs				Outputs							
A	B	C	$\overline{G}$	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
X	X	X	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	1	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0

4. (a) The state diagram of a finite state machine (FSM) is given in Figure 2.

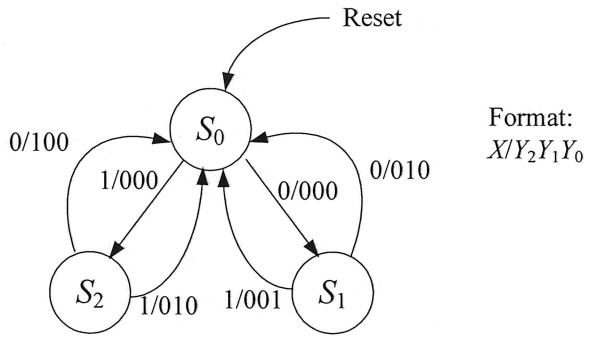

Figure 2

(i) State if the FSM is a Moore machine or a Mealy machine, and explain why.

(ii) Starting with initial state S_0, derive the output $Y_2Y_1Y_0$ for an input sequence $X = 001001111001$.

(iii) What is the likely function of the FSM?

(10 Marks)

(b) Figure 3 shows an ASYNCIN input being synchronized to the synchronous system. Explain and illustrate using timing figure the underlying problem with this mode of synchronizing an input.

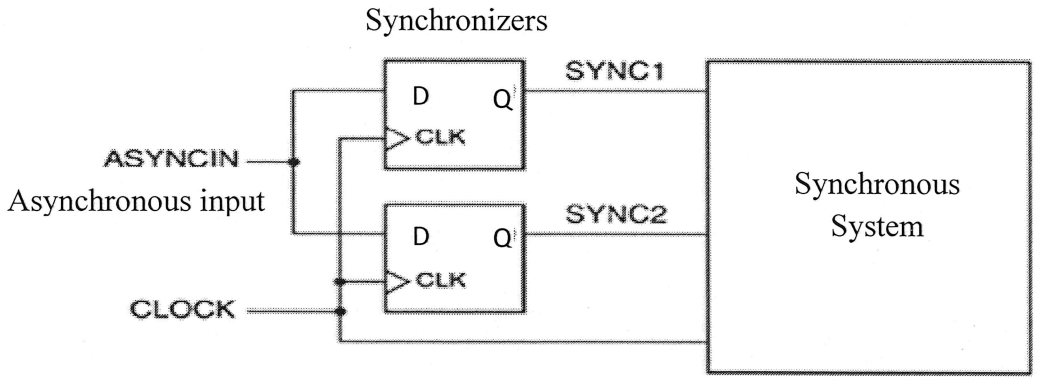

Figure 3

(6 Marks)

(c) Refer to Figure 4 (on page 6) on the chip configuration of a DRAM. State the size of the memory chip. How many of such chips will be required to realize a 1-MByte memory module?

Note: Question No. 4 continues on page 6.

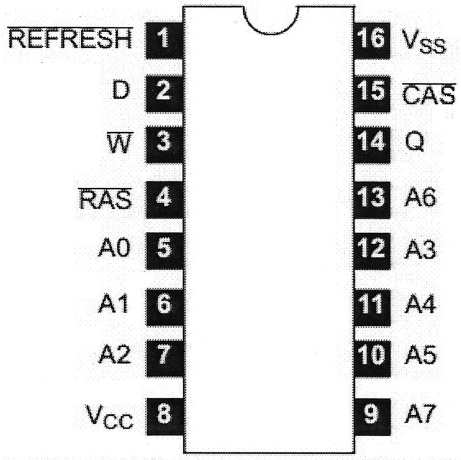

Figure 4

(4 Marks)

5. Refer to the circuit in Figure 5 and answer the following questions. In the circuit, X is an external control input, and the reset input of each flip-flop operates asynchronously.

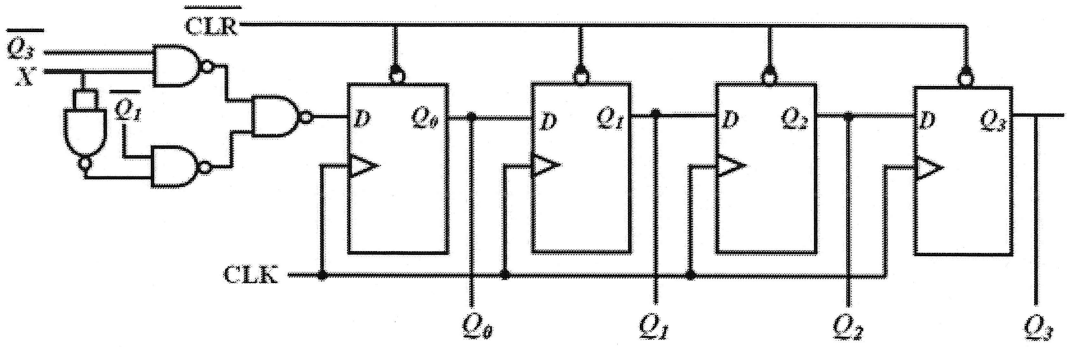

Figure 5

(a) Draw the state diagram for the circuit. In your state diagram, label the states encoding according to the format $Q_0Q_1Q_2Q_3$, meaning Q_0 written as the most significant bit while Q_3 being the least significant.

(10 Marks)

(b) Give a brief description of the function of this circuit.

(3 Marks)

(c) List down the unused states.

(3 Marks)

(d) If the maximum delay of each NAND gate is 6 ns, and the maximum delay and setup time of each flip-flop are 12 ns and 4 ns, respectively, determine the critical clock frequency of the circuit.

(4 Marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.

Matriculation Number: | | | | | | | | | |

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ANSWER SHEET FOR QUESTION NO. 3(a)

Note: This Answer Sheet is to be attached to your Answer book.

Question 3(a)

Table 2

Input				*Output*		
A_1	A_0	B_1	B_0	$Y_{A>B}$	$Y_{A=B}$	$Y_{A<B}$
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

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ANSWER SHEET FOR QUESTION NO. 3(b)

Note: **This Answer Sheet is to be attached to your Answer book.**

Question 3(b)

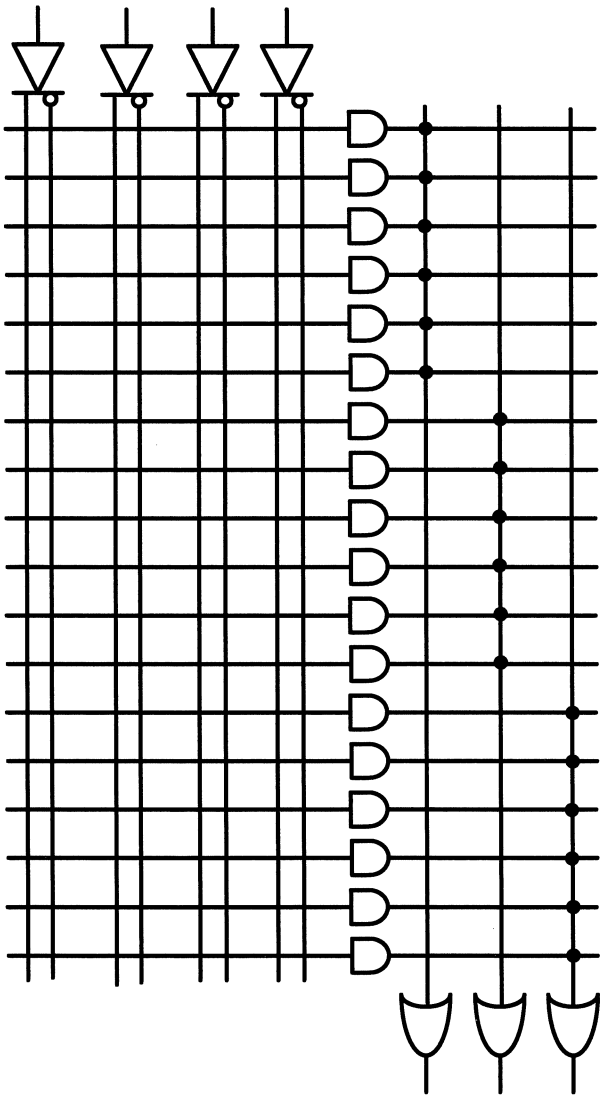

Figure 1